Design of New Power Electronic Converter(PEC) for Photovoltaic Systems and Investigation of Switches Control Technique

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Abstract— this paper proposes a new power electronic converter for photovoltaic systems applications. The proposed power electronic converter consists of multi-output DC/DC boost converter and multilevel inverter. This power electronic converter needs to minimum number of power electronic elements such as IGBTs, gate drivers, diodes and capacitors. This converter can generate all output voltage levels (odd and even) at the output voltage waveform. Fundamental frequency-switching technique is applied to the proposed topology to trigger the switches for controlling the voltage levels generated on the output. Verification of the analytical results is done using MATLAB simulation software.

***Keywords*— photovoltaic systems, multilevel inverter, multi-output, switching technique.**

I. INTRODUCTION

Limited fossil energy and increased air pollution have worried researchers to improve clean energy sources. One of these sources is the photovoltaic (PV) system, which is a quiet, clean and an efficient strategy for generating electricity [1]-[3]. Photovoltaic systems require a power electronics interface to define their operating point at optimal conditions for any load or grid-connection.

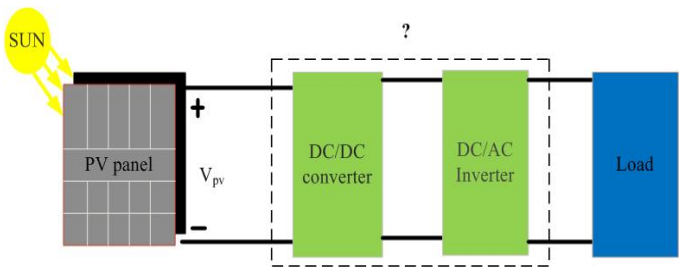


Fig. 1. The structure of photovoltaic systems.

This aspect has been addressed by single-stage inverters, or by adopting double-stage structures based on DC/DC and DC/AC converters [4], [5]. Fig. 1 shows the structure of photovoltaic systems. In this paper, the challenge is to link the DC generated voltage by the photovoltaic system with output load. DC-DC converters are used in low and high power applications [6]. Recently, several multi-output DC-DC converters have been proposed. Multi-output DC-DC converters are more efficient compared to use several separate single output power supplies [7].

Multi-output DC-DC converters are more efficient compared to use several separate single output power supplies [7]. A novel multi-output DC-DC boost converter, which can be utilized as a front-end converter to boost the inverter's dc link voltage for grid connection systems has been proposed in [8]. By the use of this converter, the dc voltage across each capacitor can be adjusted to a desired voltage level and the main problem associated with balancing the capacitors' voltages is solved.

Multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. In general, there are three kinds of multilevel inverters:

- Diode clamped inverter.
- Flying-capacitor inverter.
- Cascade H-bridge inverter.

The diode-clamped inverter utilizes capacitors in series to divide up the DC bus voltage into a set of output voltage levels. This inverter uses more number of diodes and switches. Also, the balancing of capacitors' voltages is difficult [9]. The flying-capacitor inverter utilizes a ladder structure of the DC side capacitors where the voltage on each capacitor differs

from that of the next capacitor. This structure needs a large number of capacitors and switches [10].

Cascade inverter is one of the most important topologies in comparison with other classical multilevel inverters [11]. Cascade topology requires the least number of power electronic components when compared to diode clamped and flying capacitor topology [12]. This structure consists of a number of H-bridge inverter cells with separate dc source for each cell and it is connected in series [13].

Several modulation technique have been improved for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), fundamental frequency switching and so on [14]-[18]. This paper focuses on fundamental frequency switching strategy for trigger the power electronic switches for controlling and generating output voltage levels.

II. PROPOSED POWER ELECTRONIC CONVERTER.

Fig. 2 shows the basic unit topology for proposed power electronic converter. This topology consists of two output DC-DC boost converter and 5-level inverter.

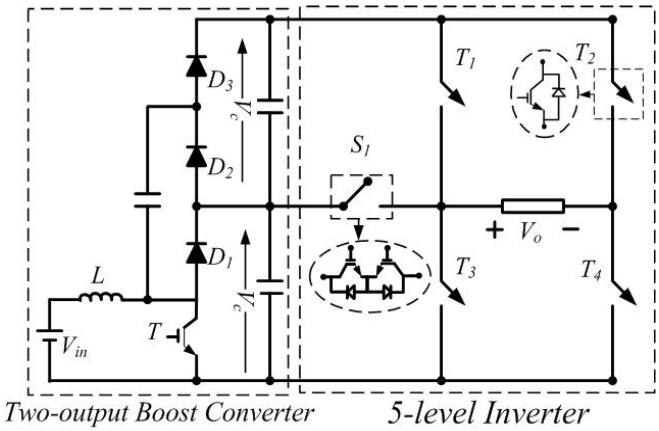
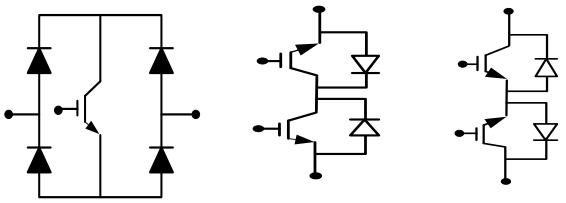


Fig. 2. Basic unit for proposed power electronic converter topology.

The performance and operation of the two-output boost converter has been investigated in [8]. The values of capacitors' voltages are equal and it is achieved using the following equation:

$$\frac{V_c}{V_{in}} = \frac{1}{1-D} \tag{1}$$

Where D represents the duty cycle of T switch. By the control of duty cycle of T switch, the voltage of each capacitor is adjusted. In this topology, the two-output DC-DC converter has connected to the 5-level inverter. The switches of 5-level inverter are unidirectional and bidirectional. In fact, the switches of full-bridge converter are unidirectional. Each unidirectional switch consists of an IGBT and an antiparallel diode. But, the S_1 switch is bidirectional. This switch can conduct current in both directions. Several structures have been designed for bidirectional switch [19]. Fig. 3 depicts a number of these structures. The switch shown in Fig. 3(a) is easy to control, but its ON-state voltage drop is high. The switch shown in Fig. 3(b) reduces the ON-state voltage drop, but requires two IGBTs. One possible restriction is that each IGBT requires an isolated gate driver, so the gate driver circuits will be expensive. Fig. 3(c) shows the common emitter structure. The conduction losses are identical to the structure shown in fig. 3(b). The advantage of this structure over the previous one is that each bidirectional switch needs a gate driver [20]. Hence, we use this structure for *T* switch.



(a) (b) (c)

Fig. 3. Different structures for bidirectional switches.

For the suggested 5-level inverter, the state of the switches for each output voltage value is shown in table I. It is noticeable that there are several switching states for generating the zero voltage level and in the Table I, only one of them is shown. In this table, 1 means that the corresponding switch is turned ON and 0 indicates the OFF state.

Table I. Output Voltage for Different States of Switches for 5-Level Inverter.

State	Switches States					Output Voltage (V_o)
	S_1	T_1	T_2	T_3	T_4	
1	0	1	1	0	0	0
2	1	0	0	0	1	V_c
3	1	0	1	0	0	$-V_c$
4	0	1	0	0	1	$2V_c$
5	0	0	1	1	0	$-2V_c$

In this topology, V_{in} is the input voltage. It is noticeable that Instead of input voltage we can use renewable energy sources such as photovoltaic systems (or fuel cells) and so on.

As the number of output voltage level increases, the output voltage waveform becomes closer and closer to a sinusoidal waveform with fewer magnitude of harmonic content. In order to increasing the number of levels in output voltage of the proposed power electronic converter, the basic unit shown in Fig. 2 can be extended as shown in Fig. 4, which called power electronic converter (PEC). The proposed PEC consists of two stages:

1) Multi-output boost converter.
2) Multilevel inverter.

The multi-output boost converter stage is an *N-output* DC–DC converter based on one driven switch, *2N-1* diodes and *2N-1* capacitors. One advantage of the structure is that the number of levels can be extended by only adding capacitors and diodes and the main circuit does not need to be modified.

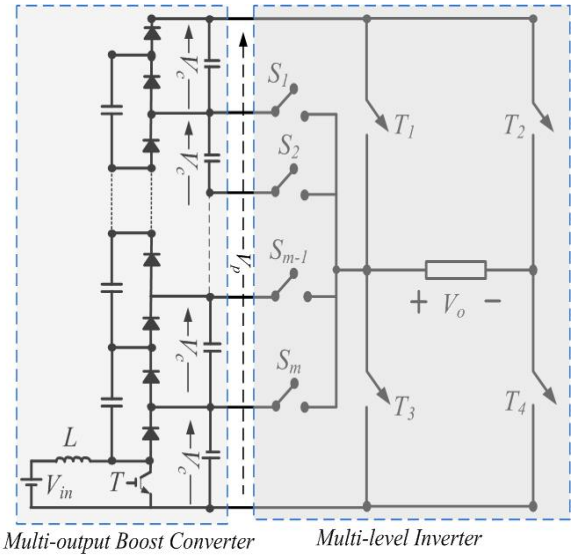


Fig. 4. Proposed power electronic converter (PEC).

In this topology, the value of output voltage of the multi-output boost converter (V_p) is obtained using the following equation:

$$\frac{V_p}{V_{in}} = \frac{N}{1-D} \tag{2}$$

The proposed multi-output boost converter has been connected to the multilevel inverter. In proposed structure, the number of output voltage levels (N_{level}) and IGBTs (N_{IGBT}) can be obtained by (3) and (4), respectively:

$$N_{level} = 2m+3 \tag{3}$$

$$N_{IGBT} = 2m+4 \tag{4}$$

In the proposed multilevel inverter topology, the structure of bidirectional switches $(S_1, S_2, \ldots, S_m)$ is composed by two switches which each switch has an anti-parallel diode and an IGBT. This structure requires only one gate driver circuit.

But, the type of switches in full-bridge converter is unidirectional. The total number of drivers (N_{driver}) is given by (5):

$$N_{driver} = m+4 \tag{5}$$

Where *m* represents the number of bidirectional switches in multilevel inverter. Considering (3) and (4), it is obvious that we have:

$$N_{IGBT} = N_{level} + 1 \tag{6}$$

The comparison between the classical multilevel inverter topologies and suggested multilevel inverter structures in terms of power electronic component requirements for an X-level $(N_{level} = X)$ output voltage is listed in Table II. The most important Part in multilevel inverters is IGBTs, which increase the cost and control complexity and tend to reduce the overall reliability and efficiency. This table shows that proposed multilevel inverter needs to minimum number of IGBTs in comparison with other classic structures. The gate driver circuits are the electronic part of the circuit and increasing the number of gate driver circuits is a considerable deficiency. Because increasing gate drivers cause increasing costs and control complexity.

It is evident that the power electronic components are reduced in the proposed topologies significantly. Also, the proposed topology don't need to clamping diodes and balancing capacitors. This comparison shows that the proposed multilevel inverter requires minimum number of power electronic components and it is the main advantage and feature of the proposed multilevel inverter. It is considerable that the capacitors' voltages (V_C) are equal. The relation between the number of gate driver circuits and levels is obtained as follows:

$$N_{driver} = \frac{\left(N_{level}+5\right)}{2} \tag{7}$$

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TABLE II. COMPARISON OF THE PROPOSED TOPOLOGIES WITH CLASSICAL MULTILEVEL INVERTER TOPOLOGIES.

Topology	Power Electronic Components				
	Clamping Diode	Balancing Capacitor	IGBT	Gate Driver	DC Bus Capacitor
Diode Clamped	$(X-1)\times(X-2)$	0	$2(X-1)$	$2(X-1)$	$(X-1)$
Flying Capacitors	0	$(X-1)\times(X-2)/2$	$2(X-1)$	$2(X-1)$	$(X-1)$
Cascaded H-bridge	0	0	$2(X-1)$	$2(X-1)$	$(X-1)/2$
Proposed Multilevel Inverter Topology	0	0	$X+1$	$(X+5)/2$	$(X-1)/2$

The gate driver circuits are the electronic part of the circuit and increasing the number of gate driver circuits is a considerable deficiency. Because increasing gate drivers cause increasing costs and control complexity. It is evident that the power electronic components are reduced in the proposed topologies significantly. Also, the proposed topology don't need to clamping diodes and balancing capacitors. This comparison shows that the proposed multilevel inverter requires minimum number of power electronic components and it is the main advantage and feature of the proposed multilevel inverter. It is considerable that the capacitors' voltages (V_C) are equal.

III. Investigation of Switches Control Technique.

The output voltage of multi-output boost converter can be controlled by the duty cycles of the T switch, which the affecting of the duty cycle of T switch on the output voltage is fully explained in [8].

To control of the switches of the proposed multilevel inverter topology $\left(S_1, S_2,\ldots, S_m, T_1, T_2, T_3, T_4\right)$, the fundamental frequency-switching strategy has been used. Because the fundamental frequency-switching strategy has its low switching frequency in comparison with other strategies and it is an advantage [21]. For power converters, the total harmonic distortion (THD) is a popular performance index, which evaluates the quantity of harmonic contents in the output waveform. For sinusoidal waveform, the THD is defined as follows:

$$\mathrm{THD}=\frac{\sqrt{\left(\sum_{n=3,5,7,\ldots}^{\infty} V_{o_n}\right)}}{V_{o_1}}=\sqrt{\left(\frac{V_{o_{rms}}}{V_{o_1}}\right)-1} \qquad (8)$$

In this equation, *n* represents the order of the corresponding harmonic, while the sub-index 1 corresponds to the fundamental frequency. Therefore, V_{o_n} and V_{o_1} are the rms of the *n* order harmonic and fundamental of the output voltage waveform, respectively. Also, $V_{o_{rms}}$ represents the rms magnitudes of the output voltage. In above equation, the magnitude of V_{o_1} and $V_{o_{rms}}$ can be calculated using the following equations, respectively:

$$V_{o_1}=\frac{2\sqrt{2}V}{\pi}\sum_{j=1}^{N_{level}}\cos\left(n\theta_j\right) \qquad (9)$$

$$V_{o_{rms}}=\frac{2\sqrt{2}V}{\pi}\sqrt{\sum_{n=1}^{\infty}\left(\sum_{j=1}^{N_{level}}\frac{\cos\left(h\theta_j\right)}{h}\right)^2} \qquad (10)$$

Where, the values of $\theta_1,\theta_2,\theta_3,\ldots,\theta_{N_{level}}$ represent switching angles and is calculated by:

$$\theta_j=\sin^{-1}\left(\frac{j-0.5}{N_{level}}\right) \quad j=1,2,\ldots,N_{level} \qquad (11)$$

Using (8-11), it is obvious that the magnitude of THD depends on the number of levels and switching angles. It is clear that increasing the number of levels leads to the multilevel inverter produces near-sinusoidal output voltage waveform and as a result, very low harmonic distortion. The objective of this paper is not the calculation of the optimal switching angles in order to the elimination of selected harmonics and reducing the total harmonic distortion (THD).

IV. Simulation Results

In order to validate the proposed power electronic converter, MATLAB-Simulink software has been utilized. In this topology studied to examine the characteristics of the output voltage and output current. The simulation studies are carried out for a 9-level converter. The parameters selected for testing are provided in table III.

TABLE III.
THE PARAMETERS SELECTED FOR PROPOSED POWER ELECTRONIC CONVERTER.

Parameter	Value
Input voltage	50V
duty cycle of the T switch	0.5
Inductor(L)	1.4mH
Capacitors(C)	100µF
The switching frequency of the T switch	100KHZ
Output voltage frequency	50HZ
Resistive load	200Ω
Inductive load	100mH

The simulation studies are carried out for two different topologies.

A. 7-Level Power Electronic Converter.

Fig.5 shows the structure of the proposed 7-level power electronic converter. The stage of inverter has been used 6 gate driver circuits and 8 IGBTs. The input voltage (V_{in}) ,lower capacitor voltage (V_C) and the output voltage of multi-output boost converter (V_p) waveforms are shown in Fig. 6. This figure show that the voltage of capacitor has boosted to 100V and the output voltage of multi-output boost converter waveforms is 300V.

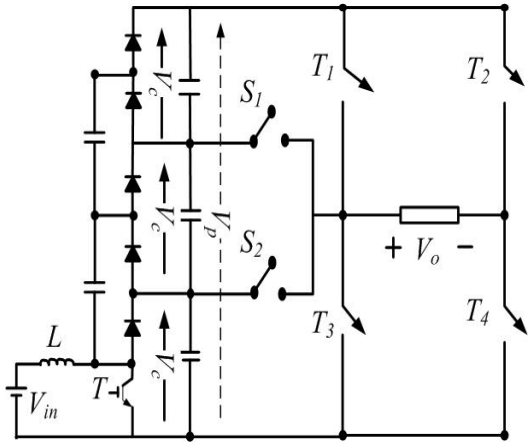
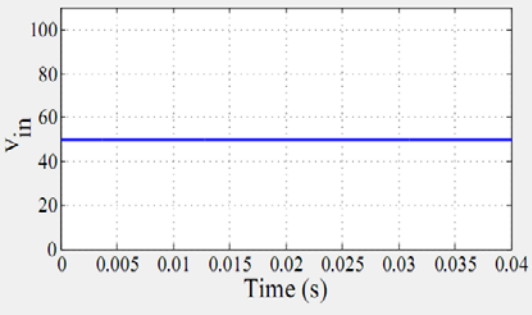


Fig. 5. Proposed 7-level power electronic converter structure.



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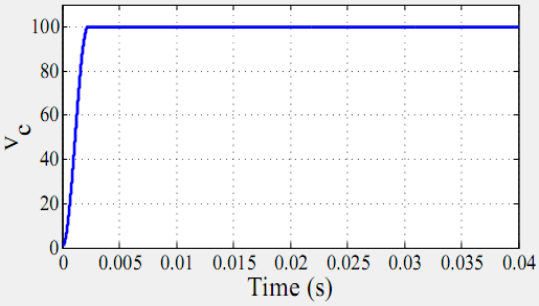

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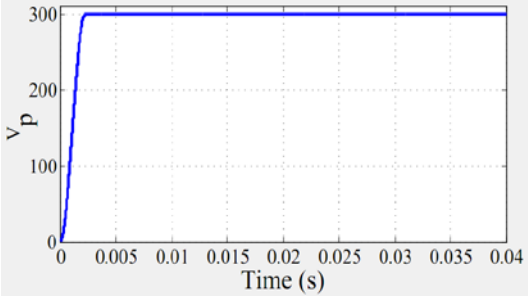


(c)

Fig. 6. (a)Input voltage (V_{in}) ;

(b) Lower capacitor voltage (V_c) ;

(c) Output voltage of multi-output boost converter (V_p) .

The output voltage and current waveforms and their corresponding Fourier spectrums are shown in Fig. 7 and 8, respectively. THD of the output voltage and current based on simulations are 10.87% and 3.37%. Based on the output current waveform and the value of THD for current, it is clear that the load current is almost sinusoidal. Because, the R-L load of the proposed converter (R-L) behaves as a low-pass filter for the current.

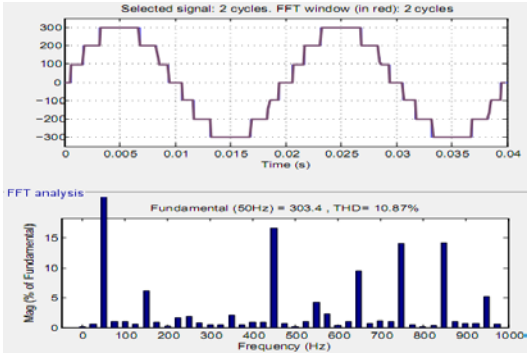


Fig. 7. Output voltage and harmonic spectrum of 7-Level power electronic converter (THD=10.87%).

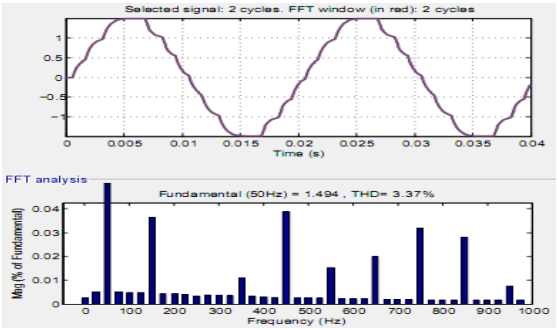


Fig. 8. Output current and harmonic spectrum of 7-level power electronic converter (THD=3.37%).

B. 9-Level Power Electronic Converter.

The structure of the proposed 9-level power electronic converter is shown in fig. 9. The stage of inverter has used 7 gate driver circuits and 10 IGBTs.

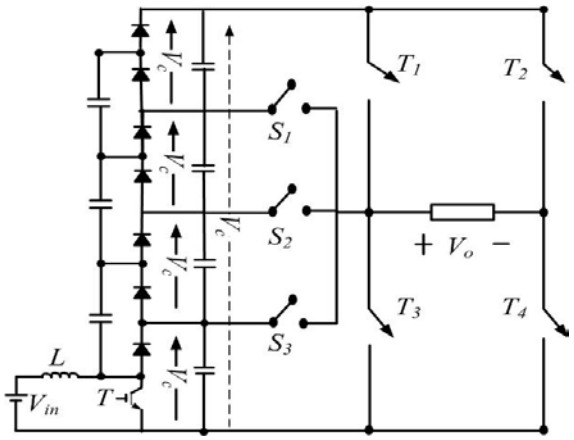
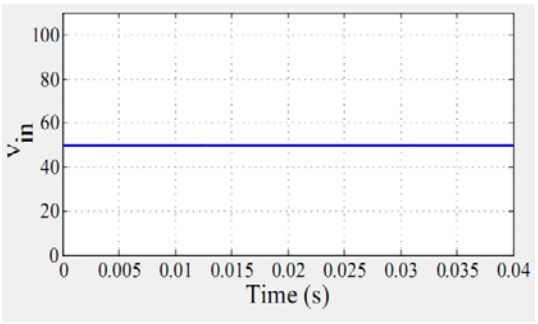
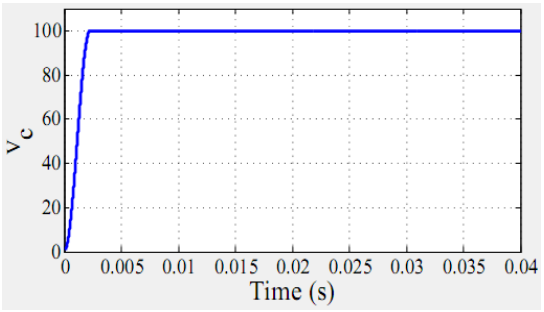


Fig.9. Proposed 9-level power electronic converter structure.

For this topology, the input voltage (V_{in}) ,lower capacitor voltage (V_c) and the output voltage of multi-output boost converter (V_p) waveforms are shown in Fig. 10. This figures show that the input voltage and lower capacitor voltage are 50V and 100V, respectively. Also, the value of the voltage of 4-output boost converter is 400V.



(a)



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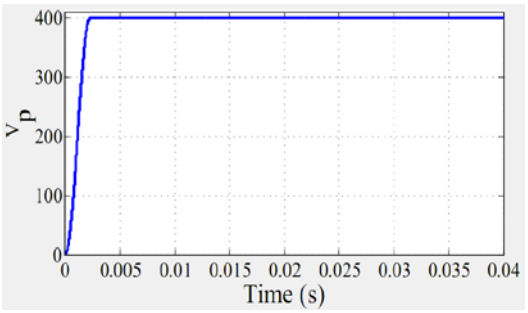

(c)

Fig. 10. (a)Input voltage (V_{in}) ;

(b) Lower capacitor voltage (V_c) ;

(c) Output voltage of multi-output boost converter (V_p) .

The load voltage and current waveforms and their corresponding Fourier spectrums are shown in fig. 11 and 12, respectively. THD of the output voltage and current based on simulations are 8.17% and 2.54%. The comparison of THDs of output voltage and current in two topologies show that increasing the number of levels leads to the proposed power electronic converter generates output voltage waveform with very low THD, which a good correspondence with the definition of THD. For increasing high power quality and desired output voltage waveform, other switching strategy should be applied to the converter or the number of voltage levels should be increased.

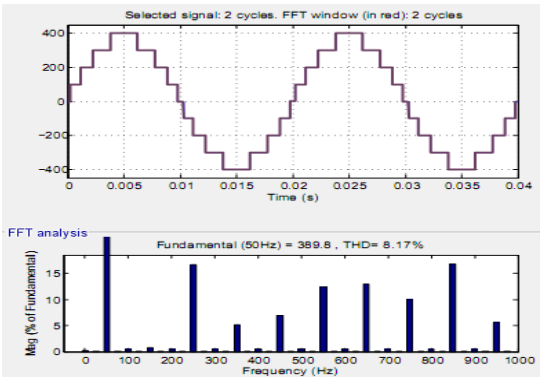

Fig. 11. Output voltage and harmonic spectrum of 9-Level power electronic converter (THD=8.17%).

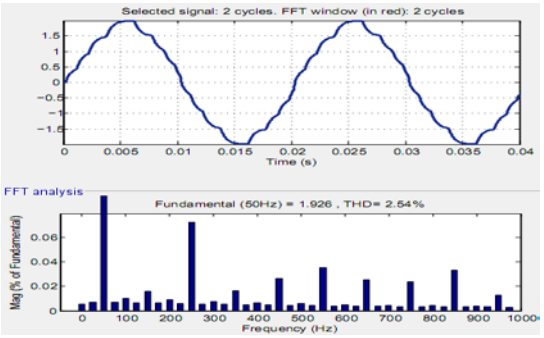

Fig. 12. Output current and harmonic spectrum of 9-level power electronic converter (THD=2.54%).

V. CONCLUSION

In this paper, a new power electronic converter for photovoltaic systems application was presented. This converter can increase the value of the generated voltage by the photovoltaic system using multi-output DC-DC boost converter. The proposed multilevel inverter can generate more number of levels with reduced number of power electronic elements. For proposed multilevel converter, the fundamental frequency-switching strategy was applied to trigger the switches for generating the voltage levels on the output. The operation of the recommended power electronic converter has been verified by simulation results for two topologies.

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